REMARKS

Claim 1 and paragraphs 0016 and 0017 of the specification have been amended. Claims 21-34 have been added. No new matter has been added.

Regarding the objection to the drawings under 37 C.F.R. 1.83(a), proposed drawing changes are indicated in red on the attached marked-up versions of Figure 1 and Figure 2. Referring to Figure 1, an exemplary wire bond 44 is shown coupled between peripheral component circuit 24 and pins 30 as disclosed by paragraph 0016 of the specification. Referring to the attached Figure 2, shading has been added to better represent gel material 42.

Regarding the objection to claim 1 for an informality, claim 1 has been amended and is thought to be in correct form. Specifically, "interconnect locations" has been replaced with "interconnects," which properly identifies a structure to which pins may be coupled by a wire bond.

Regarding the rejection of claim 1 under 35 U.S.C. §112, first paragraph, paragraphs 0016 and 0017 of the specification have been amended to include the recitations regarding bottomless cover 26 and bottom section 28 called for by claim 1, thus providing proper enablement for claim 1. The recitations of claim 1 presently incorporated into paragraphs 0016 and 0017 of the specification were included in the originally filed claim 1. Specifically, claim 1 recites that the cover is made of a material having the capability of withstanding high temperatures; therefore, the recitation was added to paragraph 0016 in describing bottomless cover 26 of housing 10. Additionally, claim 1 includes the recitation that the bottom is made from a material having heat sink capabilities; therefore, the recitation was added to paragraph 0017 in describing bottom section 28 of housing 10. No new matter has been added.

Regarding the rejection of claims 1 and 4-5 under 35 U.S.C. §103(a) over Buselmeier et al., U.S. Patent No. 4,792,878, Buselmeier et al. discloses a heat dissipating housing for integrated circuit IC and diode D (Figures 2 and 4; column 3, lines 51-63; column 4, lines 3-20). Referring to Figure 4 of Buselmeier, cover W and bottom tub G form a first housing, and secondary housing SI/E houses light-emitting diode D (Figure 1; column 4, lines 14-15). Diode D appears to be connected by lines Z (Figure 2; column 4, lines 21-27) to driver chip IC. Plug pins KP appear to be supported by tub G. Printed

circuit board LP includes holes which receive plug pins KP (column 3, lines 40-43), apparently providing conductivity with driver chip IC.

In contrast to Buselmeier et al., claim 1 calls for an assembly having a cover and a bottom, the bottom being made from a material having heat sink capabilities and having a plurality of interconnect pins molded therein, the pins being coupled to interconnects of at least one hybrid circuit by wire bond, and the interconnects being at an open side of the cover.

Buselmeier does not disclose, teach or suggest a hybrid circuit having interconnects at an open side of a cover. Rather, Buselmeier discloses a diode D having terminals extending from a secondary housing SI/E and well within the cavity formed by cover W (Fig. 2). An apparent second level of conductivity is taught in that pins KP are received by circuit board LP, upon which driver chip IC is mounted. Additionally, Buselmeier does not disclose, teach or suggest pins being coupled to interconnects of at least one hybrid circuit by wire bond. Rather, Buselmeier discloses diode D being connected by line Z to another circuit including driver chip IC (column 4, lines 21-27).

Buselmeier also does not disclose, teach, or suggest a bottom being constructed of a material having heat sink capabilities. In contrast, column 3, lines 60-63 state that "cooling occurs only via the cover W and to a very limited extent via the other surfaces G/G1."

The assembly taught by Buselmeier contains multiple housings and separate circuit components (IC and D) that must be coupled together, leading to the redundant packaging, complexity, and risk of lower reliability that the present invention sought to overcome (paragraph 0004). Advantageously, the heat sink assembly called for by Applicants' amended claim 1 provides increased overall circuit density and reduces valuable packaging space, overcoming the complexity, high cost, and increased risk of poor reliability in prior art heat sink assemblies such as that disclosed by Buselmeier.

Applicants respectfully submit that claims 1-7 and 20 as amended are not disclosed by nor obvious over Buselmeier et al. and are therefore in condition for allowance.

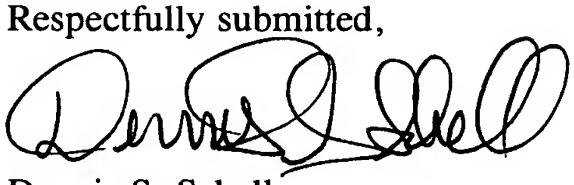
In view of the foregoing, Applicants submit that the application, as amended, is in condition for allowance, and such favorable action is respectfully requested.

Applicants submit herewith a check in the amount of $36.00 as payment for two additional claims. In the event any extension of time or additional payment of fee is

required, Applicants hereby conditionally petition therefore and authorize any charges to be made to Deposit Account No. 02-0390, BAKER & DANIELS.

Should the Examiner have any questions or suggestions which would expedite the prosecution of this application, the Examiner is invited to telephone Kevin R. Erdman at (317) 237-1029.

Respectfully submitted,



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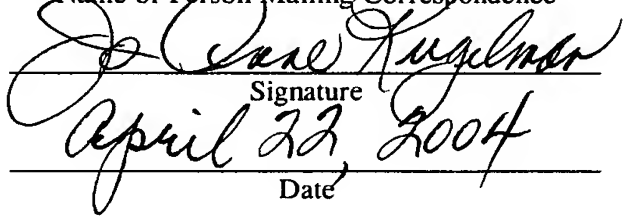

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April 22, 2004
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